IN THE CLAIMS

1. (currently amended) An integrated circuit (IC) for data communication comprising:

a digital signal processor;

circuitry for receiving digital signals from physical layer devices within a communication network;

circuitry for receiving analog signals from a selected one of said physical layer devices;

circuitry for routing said analog and digital signals to [[a]] said digital signal processor (DSP), said DSP outputting processed signals in response to DSP programming commands;

circuitry for incorporating particular processed digital signals into data packets corresponding to a communication protocol; and

circuitry for receiving and transmitting said data packets of a communication protocol to and from a network coupling said physical layer devices.

2. (original) The IC of claim 1 further comprising circuitry for outputting analog signals derived from particular ones of said processed signals from said DSP to a particular one of said physical layer devices.

3. (original) The IC of claim 1, wherein said DSP receives digital data not derived from a corresponding analog signal.

4. (original) The IC of claim 1, wherein selected first digital data from said DSP are analyzed by a network processor to determine a characteristic of said first digital data,

said characteristic used in said network processor to direct a dispensation of said first digital data.

5. (original) The IC of claim 4, wherein said processing to determine said characteristic of said first digital data comprises a pattern recognition algorithm.

6. (currently amended) A network processor integrated circuit (IC) comprising:

an embedded processor complex (EPC) with multiple processors implemented in the IC;

a first communication interface from the IC to physical layer devices;

a second interface from the IC to a switch fabric;

a memory storage unit implemented in the IC;

a digital signal processor (DSP), implemented in the IC, having an analog I/O and a digital I/O interface; and

a bus system for coupling said EPC, said physical layer devices, said switch fabric, said storage unit and said DSP.

7. (currently amended) The network processor IC of claim 6, wherein said DSP is one of said multiple processors in said EPC.

8. (currently amended) The network processor IC of claim 6, wherein said DSP is a functional core integrated into each one of multiple processors in said EPC.

9. (currently amended) The network processor IC of claim 6, wherein said DSP is a functional core external to said EPC, said DSP coupled to said EPC and to one of said physical layer devices.

10. (currently amended) The network processor IC of claim 6, wherein said DSP has an analog signal interface for receiving and sending analog signals and a digital signal interface for sending and receiving digital signals.

11. (currently amended) The network processor IC of claim 6, wherein said DSP receives program commands via said switch fabric from a remote device.

12. (currently amended) The network processor IC of claim 6, wherein said DSP receives program commands via a general purpose processor in said network processor IC.

13. (currently amended) A method for improving the performance and functionality of a network processor integrated circuit (IC) controlling the communication between physical layer devices comprising the steps of:

adding a DSP core to said network processor IC;

coupling digital signals to and from said network processor IC and said DSP core;

executing instructions by said DSP to determine a characteristic of said digital signals; and

directing a dispensation of said digital signals based on said determined characteristic.

14. (currently amended) The method of claim 13 further comprising the steps of:

coupling analog signals to said DSP core;

digitizing said analog signals;

processing said digitized analog signals by said DSP core;

incorporating said processed digital signals into data packets corresponding to a communication protocol; and

receiving and transmitting said data packets of said processed digital signals to said physical layer devices on a communication network coupled to said network processor IC.

15. (original) The method of claim 14 further comprising the step of:

outputting analog signals converted from said processed digital signals to a particular physical layer device.

16. (currently amended) The method of claim 13, wherein said DSP core is one of multiple processors in an embedded processor complex in said network processor IC.

17. (currently amended) The method of claim 13, wherein said DSP core is a functional core integrated into one of multiple processors in a embedded processor complex in said network processor IC.

18. (currently amended) The method of claim 13, wherein said DSP core is a functional core coupled to an embedded processor complex in said network processor IC and one of said physical layer devices.

19. (original) The method of claim 13, wherein said DSP core has an analog signal interface for receiving and sending analog signals and a digital signal interface for sending and receiving digital signals.

20. (currently amended) The method of claim 13, wherein said DSP core receives program commands via a switch fabric coupled to said network processor IC from a remote device.

21. (currently amended) The method of claim 13, wherein said DSP core receives program commands via a general purpose processor in said network processor IC.